AD-A101 663 TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA --ETC F/G 9/5
GAAS ANALOG INTEGRATED CIRCUITS FOR MICROWAVE APPLICATIONS.(U)
MAY 81 N00014-81-C-0042
UNCLASSIFIED S/N-37362 NL

END
DATE FILMED
8-81
DTIC

29 May 1981

LEVEL II

(12)

(15) N00014-81-C-0042
S/N-37362

(11)

12

AD A101663

# GaAs ANALOG INTEGRATED CIRCUITS FOR MICROWAVE APPLICATIONS

(9) STATUS REPORT

FOR

April 1, 1981 - May 31, 1981

Defense and Space Systems Group of
TRW Inc.
Electronic Systems Division
Redondo Beach, CA 90278

Prepared for

Office of Naval Research

Arlington, Virginia 22217

DTIC FILE COPY

| Accession For | |
|---|---|
| NTIS GRA&I | X |
| DTIC TAB | ☐ |
| Unannounced | ☐ |
| Justification | |
| By Per Ltr. on File | |
| Distribution/ | |
| Availability Codes | |
| Dist | Avail and/or Special |
| A | |

DTIC
ELECTE
JUL 21 1981
S D
D

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

412419

81 6 22 118

## 1.0 OBJECTIVE OF PROGRAM PHASE I

The objective of the first phase of the GaAs Analog Integrated Circuits program is to develop several monolithic circuits which can be used as building blocks in a $360^{\circ}$ continuously variable phase shifter. The circuits are to be designed, fabricated and tested to determine how they will perform in a hybrid and later a completely monolithic phase shifter. The circuits required include microwave analog multipliers at 10 GHz, a quadrature phase splitter and appropriate input and output circuits.

## 2.0 SUMMARY OF ACTIVITIES TO DATE

- Phase I contract work began 13 April 1981. Some preliminary work was begun before this date.
- Modeling of a single gate FET for use in the input balun was completed.
- A $90^{\circ}$ highpass-lowpass balanced phase shifter was designed.
- An alternate $90^{\circ}$ lumped element hybrid was designed.
- Design of the input balun was nearly completed.

## 3.0 PROGRESS DURING THIS REPORTING PERIOD

A single gate FET was chosen for use in the input balun. The circuit was then designed using the measured S-parameters. A highpass-lowpass phase shifter has been designed and will be fabricated as one building block. The balun and phase shifter function as a quadrature phase splitter. An alternate approach has also been designed. It consists of a lumped element equivalent of a branched line coupler. It would be followed by two balun circuits for creating the balanced inputs to the multipliers.

## 3.1 Single Gate FET

A pair of single gate FETs is required for the design of the input balun. They must have reasonable gain at 10 GHz and be well matched. Such devices are currently being fabricated and rf characterized. Therefore, the design will be based on a device from a wafer processed with the standard IC procedure.

S-parameters for six devices from wafer RFI-35 were averaged and the bond wire inductance removed. The resulting S-parameters are given in Table 1. Table 2 lists a summary of amplifier characteristics for the composite device. Notice that the device is conditionally stable with a maximum stable gain of 10 dB at 10 GHz.

## 3.2 Highpass - Lowpass $90^{o}$ Phase Shifter

A highpass pi filter was designed which will advance the phase of a signal by $45^{o}$. The lowpass pi filter retards phase by $45^{o}$. The difference between the two outputs is $90^{o}$. The final design is shown in Figure 1. The component values are dependent on the external impedance required. In this case the output impedance was chosen as 50Ω. Other values of impedance result in smaller values of the shunt capacitance or larger values of the shunt inductance. For the 50Ω configuration, all the component values can be easily obtained except for the .13pF capacitor. This value is quite small for the metal-oxide-metal type of capacitor fabricated with the standard process. The capacitance may have to be realized using an interdigitated design. The decision will be made during layout of the circuit. Some data for interdigitated capacitors will be available by then.

The filter design produces a very uniform phase shifter over the band. Figure 2 illustrates the phase shift as a function of frequency for two cases. An inductor Q of 9 at 10 GHz has been measured for square spiral inductors fabricated with the

RF1-35 Vd=3 Id=50%Idss=52±2mA

11:16:40 2 APR 81

| FREQUENCY | REFL COEFF -IN S11 | | LOSS-FORWARD S21 | | LOSS-REVERSE S12 | | REFL COEFF -OUT S22 | |
|---|---|---|---|---|---|---|---|---|
| MHz | MAG | ANG | MAG | ANG | MAG | ANG | MAG | ANG |
| 2000.0000 | .968 | -28.3 | 1.822 | 157.3 | .023 | 72.5 | .801 | -8.6 |
| 2500.0000 | .961 | -34.5 | 1.830 | 154.6 | .029 | 72.5 | .794 | -9.6 |
| 3000.0000 | .957 | -41.4 | 1.755 | 149.5 | .034 | 66.6 | .792 | -12.0 |
| 3500.0000 | .943 | -48.0 | 1.609 | 145.2 | .038 | 66.5 | .784 | -14.6 |
| 4000.0000 | .940 | -53.4 | 1.488 | 138.2 | .041 | 59.2 | .790 | -17.8 |
| 4500.0000 | .924 | -58.4 | 1.323 | 131.5 | .043 | 55.1 | .791 | -19.7 |
| 5000.0000 | .917 | -62.6 | 1.335 | 127.5 | .047 | 51.2 | .783 | -21.1 |
| 5500.0000 | .911 | -68.0 | 1.271 | 121.4 | .052 | 45.8 | .782 | -22.6 |
| 6000.0000 | .878 | -72.8 | 1.192 | 115.1 | .062 | 31.4 | .767 | -25.9 |
| 6500.0000 | .876 | -73.0 | 1.186 | 113.0 | .044 | 36.7 | .781 | -24.9 |
| 7000.0000 | .879 | -76.9 | 1.206 | 104.7 | .055 | 36.6 | .788 | -27.4 |
| 7500.0000 | .880 | -80.9 | 1.221 | 103.5 | .057 | 33.8 | .780 | -28.3 |
| 8000.0000 | .876 | -84.1 | 1.200 | 99.9 | .066 | 31.6 | .793 | -31.6 |
| 8500.0000 | .872 | -86.4 | 1.134 | 97.7 | .073 | 31.5 | .795 | -33.4 |
| 9000.0000 | .869 | -88.9 | 1.105 | 93.6 | .081 | 28.5 | .802 | -35.7 |
| 9500.0000 | .850 | -90.4 | .964 | 89.7 | .086 | 27.4 | .809 | -36.9 |
| 10000.0000 | .857 | -92.0 | .962 | 90.4 | .097 | 26.6 | .820 | -39.5 |
| 10500.0000 | .828 | -93.8 | .885 | 81.6 | .102 | 25.5 | .826 | -40.5 |
| 11000.0000 | .814 | -94.5 | .844 | 80.0 | .115 | 26.2 | .842 | -42.0 |
| 11500.0000 | .794 | -95.0 | .809 | 74.0 | .125 | 24.9 | .849 | -43.2 |
| 12000.0000 | .771 | -95.0 | .770 | 72.5 | .132 | 25.4 | .860 | -44.2 |
| 12500.0000 | .732 | -96.3 | .772 | 67.4 | .136 | 25.1 | .866 | -44.0 |
| 13000.0000 | .658 | -99.9 | .778 | 58.8 | .132 | 24.1 | .859 | -43.1 |
| 13500.0000 | .628 | -103.6 | .751 | 59.6 | .139 | 26.5 | .868 | -42.6 |
| 14000.0000 | .574 | -108.1 | .795 | 53.5 | .150 | 22.6 | .865 | -44.0 |
| 14500.0000 | .534 | -108.7 | .735 | 46.7 | .155 | 22.3 | .860 | -44.4 |
| 15000.0000 | .485 | -108.8 | .693 | 41.8 | .160 | 22.2 | .857 | -45.0 |
| 15500.0000 | .422 | -109.3 | .705 | 36.1 | .164 | 22.6 | .857 | -45.3 |
| 16000.0000 | .314 | -108.6 | .688 | 29.4 | .167 | 25.4 | .866 | -45.2 |
| 16500.0000 | .176 | -105.2 | .735 | 21.0 | .166 | 22.1 | .857 | -45.3 |
| 17000.0000 | .056 | -81.4 | .716 | 11.8 | .163 | 24.0 | .850 | -44.8 |
| 17500.0000 | .091 | 15.8 | .707 | 6.4 | .168 | 22.0 | .837 | -45.1 |
| 18000.0000 | .182 | 23.2 | .700 | -2.2 | .165 | 24.2 | .827 | -45.5 |

Table 1. S-Parameters Averaged for Six Devices.
Bond Wire Inductance Removed.

RF1-35 Vd=3 Id=50%Idss=52±2mA

| FREQ (MHz) | Ga MAX OR MSG* (dB) | Gu MAX (dB) | S21 (dB) | K MAG |
|---|---|---|---|---|
| 2000.000 | 18.99* | 21.70 | 5.21 | .34 |
| 2500.000 | 18.01* | 20.72 | 5.25 | .28 |
| 3000.000 | 17.10* | 19.94 | 4.88 | .27 |
| 3500.000 | 16.3[illegible]* | 17.87 | 4.13 | .32 |
| [illegible]000.000 | 15.60* | 17.06 | 3.45 | .41 |
| 4500.000 | 14.92* | 15.05 | 2.43 | .58 |
| 5000.000 | 14.58* | 14.61 | 2.51 | .62 |
| 5500.000 | 13.91* | 13.87 | 2.08 | .69 |
| 6000.000 | 12.86* | 11.78 | 1.53 | .96 |
| 6500.000 | 11.91 | 11.91 | 1.48 | 1.16 |
| 7000.000 | 13.44* | 12.26 | 1.63 | .97 |
| 7500.000 | 13.28* | 12.26 | 1.73 | .94 |
| [illegible]000.000 | 12.59* | 12.21 | 1.59 | .85 |
| 8500.000 | 11.94* | 11.65 | 1.09 | .82 |
| 9000.000 | 11.34* | 11.43 | .87 | .81 |
| 9500.000 | 10.48* | 9.86 | -.32 | .92 |
| 10000.000 | 9.97* | 10.26 | -.34 | .77 |
| 10500.000 | 9.40* | 8.93 | -1.06 | .93 |
| 11000.000 | 8.67* | 8.62 | -1.48 | .87 |
| 11500.000 | 8.11* | 8.02 | -1.84 | .93 |
| 12[illegible]00.000 | 7.65* | 7.50 | -2.27 | .93 |
| 12500.000 | 7.53* | 7.10 | -2.25 | .99 |
| 13000.000 | 5.22 | 6.09 | -2.18 | 1.17 |
| 13500.000 | 5.38 | 5.76 | -2.49 | 1.10 |
| 14000.000 | 5.32 | 5.72 | -1.99 | 1.10 |
| 14500.000 | 3.96 | 4.62 | -2.67 | 1.22 |
| 15000.000 | 3.09 | 3.75 | -3.19 | 1.30 |
| 15[illegible]0.000 | 3.03 | 3.58 | -3.03 | 1.31 |
| 16000.000 | 2.99 | 3.22 | -3.25 | 1.28 |
| 16500.000 | 3.40 | 3.23 | -2.67 | 1.26 |
| 17000.000 | 3.21 | 2.69 | -2.90 | 1.29 |
| 17500.000 | 3.14 | 2.26 | -3.01 | 1.26 |
| 18000.000 | 3.11 | 2.04 | -3.10 | 1.28 |

Table 2. Summary of Amplifier Characteristics Derived From S-Parameters of Table 1.

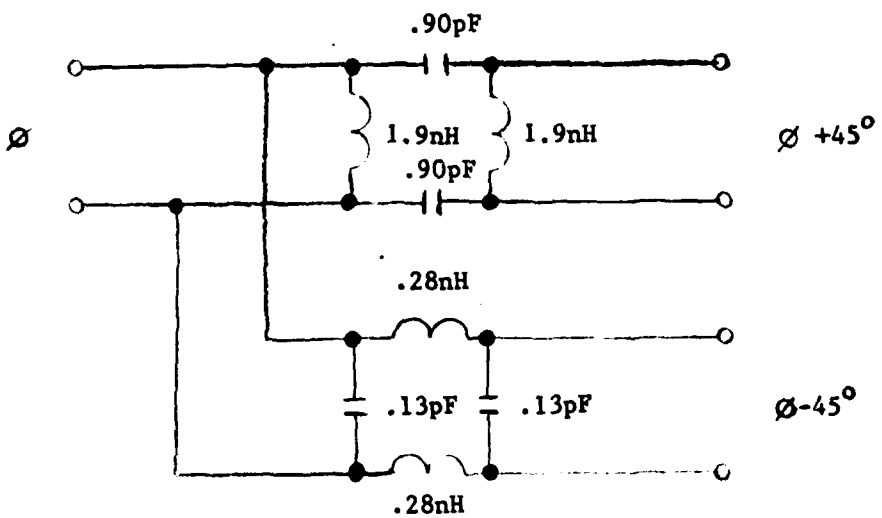



Figure 1. Highpass-Lowpass Phase Shifter for 10 GHz

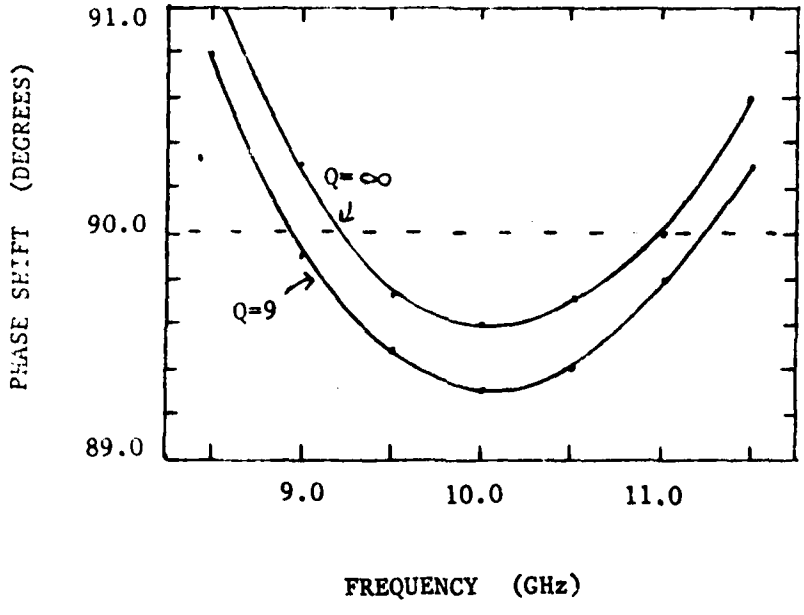



Figure 2. Highpass-Lowpass Phase Shift

standard process. With such inductors the phase shift is within 0.7° of 90° across the 9-11 GHz band. If the Q can be improved, it will increase the phase shift by less than 0.3 as shown by the limit ($Q=\infty$) also plotted in Figure 2.

The insertion loss is affected by the inductor Q as shown in Figure 3. With perfect inductors, the power at either port is virtually -3 dB of the input power. Figure 3 shows that the insertion loss with Q=9 is .35 to .5 dB. Thus the output remains flat even with the losses of the inductors included.

3.3 Lumped Element 90° Hybrid

The highpass-lowpass phase shifter is designed for real input and output impedances. If the source or load impedance deviates from the nominal value, the circuit provides little isolation between ports. An alternative is provided by a 90° hybrid which has one isolation port. The hybrid is a lumped element equivalent of a branch line coupler. The circuit is shown in Figure 4. A signal at the input is divided into two single ended outputs which are 90° apart. To be used in a phase shifter design, port 1 and port 2 would be followed by a balun circuit to provide the balanced signals to the multipliers. Although such a design requires three more FETs for a second balun, the balun output could be matched directly to the input of the multiplier rather than to the characteristic impedance of the phase shifting network. The use of a 90° hybrid and two balun circuits would result in a lower VSWR on the input of the phase shifter.

The phase shift characteristics of the hybrid are not as good as for the highpass-lowpass scheme. Figure 5 shows the phase shift for perfect and imperfect Q coils. Note how the performance is degraded as the Q decreases. The isolation provided by the circuit also comes at the expense of more insertion loss than for the

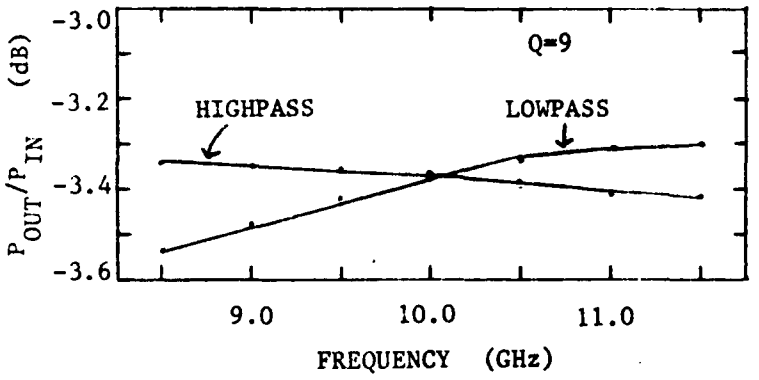



Figure 3. Highpass-Lowpass Phase Shifter Insertion Loss

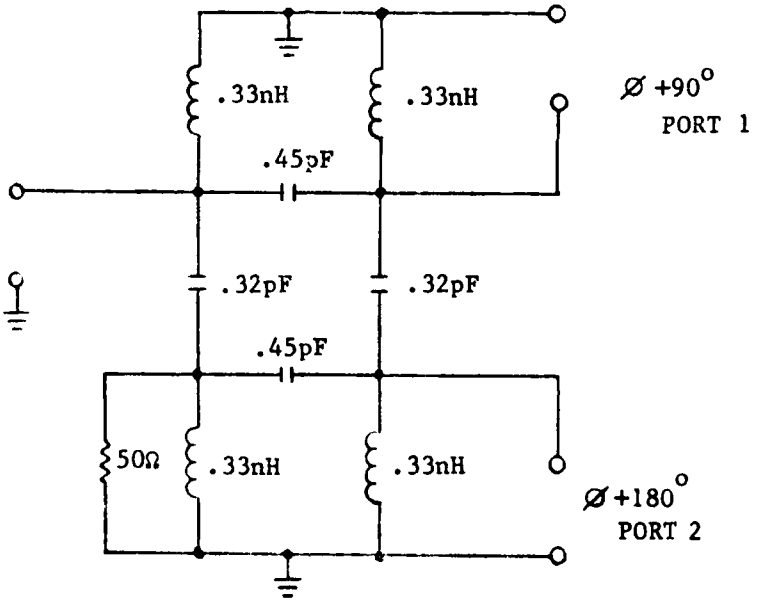



Figure 4. 90 Degree Hybrid

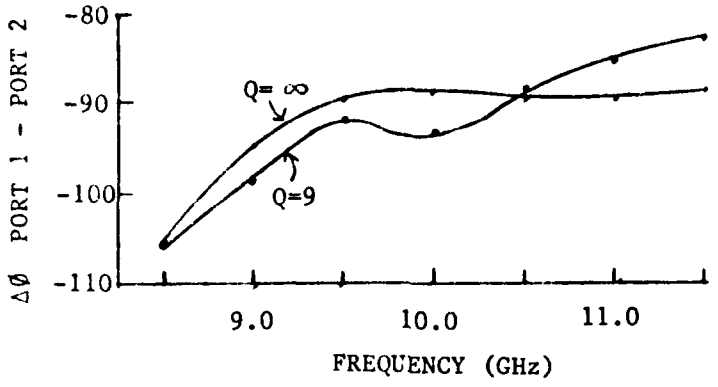



Figure 5. Phase Shift of Lumped Element 90 Degree Hybrid

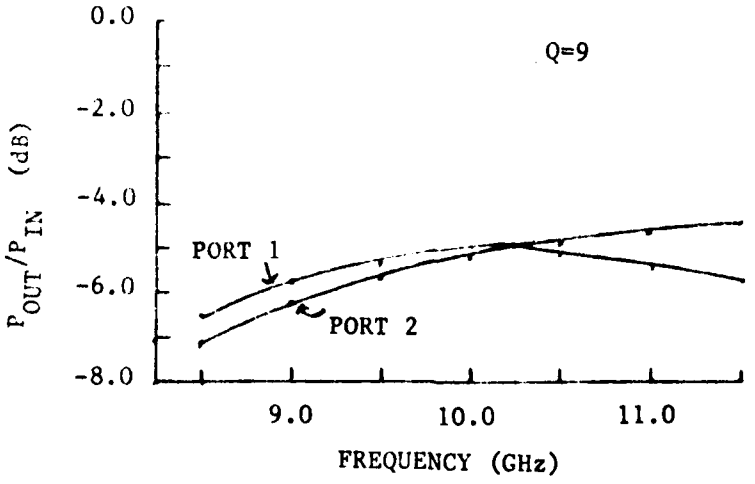



Figure 6. Insertion Loss of Lumped Element 90 Degree Hybrid

highpass-lowpass design. Figure 6 shows the calculated insertion loss at each port for an inductor Q of 9 at 10 GHz. The loss at each port is about 2-3 dB below the lossless case. Because the performance of the $90^{o}$ hybrid is not as good as the highpass-lowpass design, the hybrid will be considered as an alternate design and will be included in the building block mask set if space is available.

3.4 Input balun

The input balun converts a 50Ω single ended to a balanced 25Ω signal which can feed the highpass-lowpass phase shift circuit. The circuit has been designed using the single gate FET device data. Because the circuit has a balanced output, it must be analyzed in pieces using COMPACT. The program optimizes the matching circuits across the band or can be used to flatten the gain across the band. The pieces of circuit can then be combined and analyzed using SPICE, a second CAD program which does not optimize component values. The COMPACT calculations indicate that the balun should have about 4 dB of gain and a gain variation of 1.5 dB across the band. The circuit will be analyzed next using SPICE to confirm these numbers.

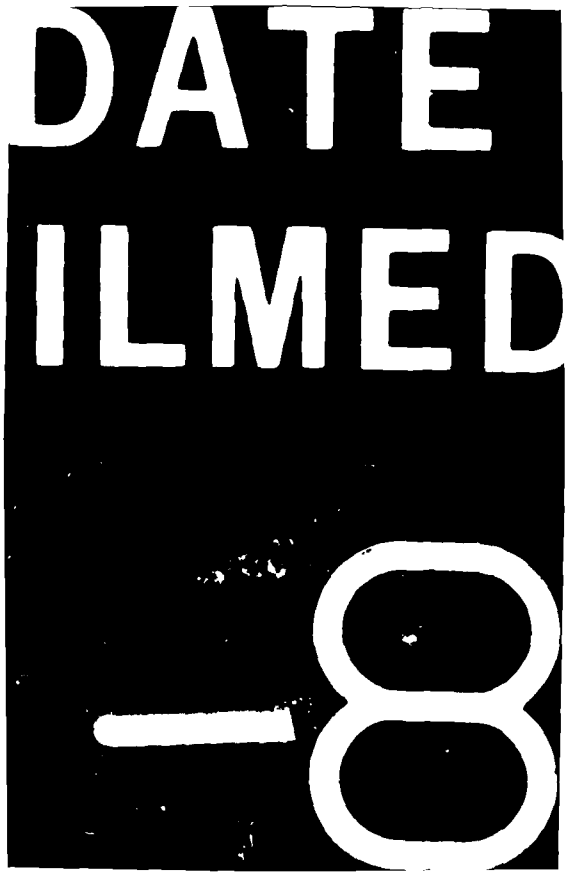
4.0 PLANS FOR JUNE 1 - JULY 31, 1981

- The input balun circuit design will be completed by checking the current design on SPICE.
- Dual gate FETs have been fabricated and will be rf characterized for the multiplier design.
- The multiplier circuit will be designed.
- Layout of the mask set will begin.

5.0 FINANCIAL STATUS AS OF 29 May 1981

Planned Expenditures - $12.9K

Actual Expenditures - $10.8K


DATE
ILMED
-8